Fig_1

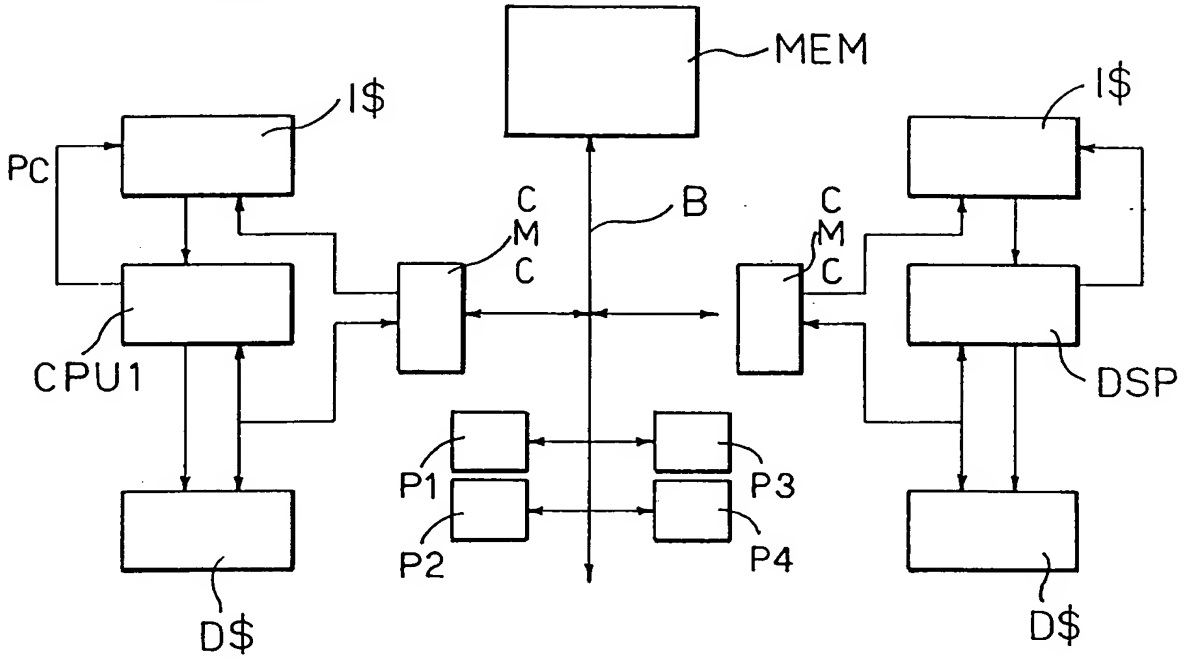
MEM
I$
I$
PC
C
M
C
B
C
M
C
CPU1
DSP
P1
P3
P2
P4
D$
D$

Fig_2

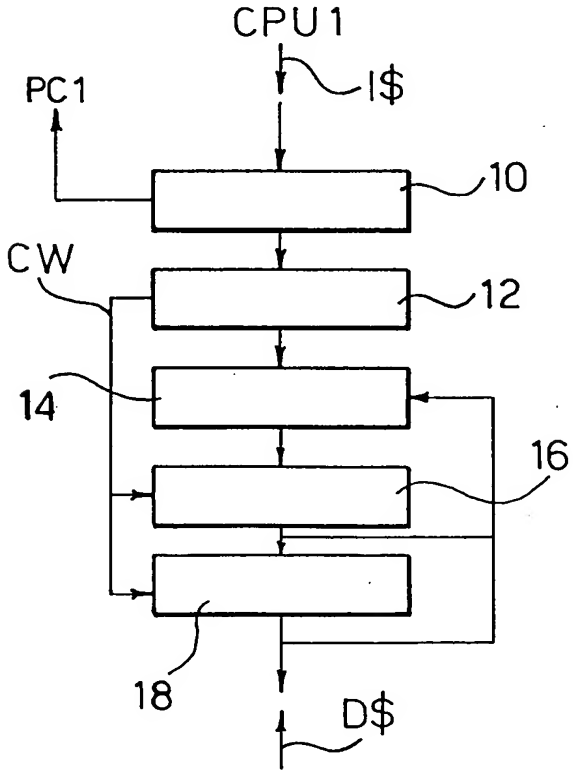
CPU1
I$
PC1
10
CW
12
14
16
18
D$

Fig_3

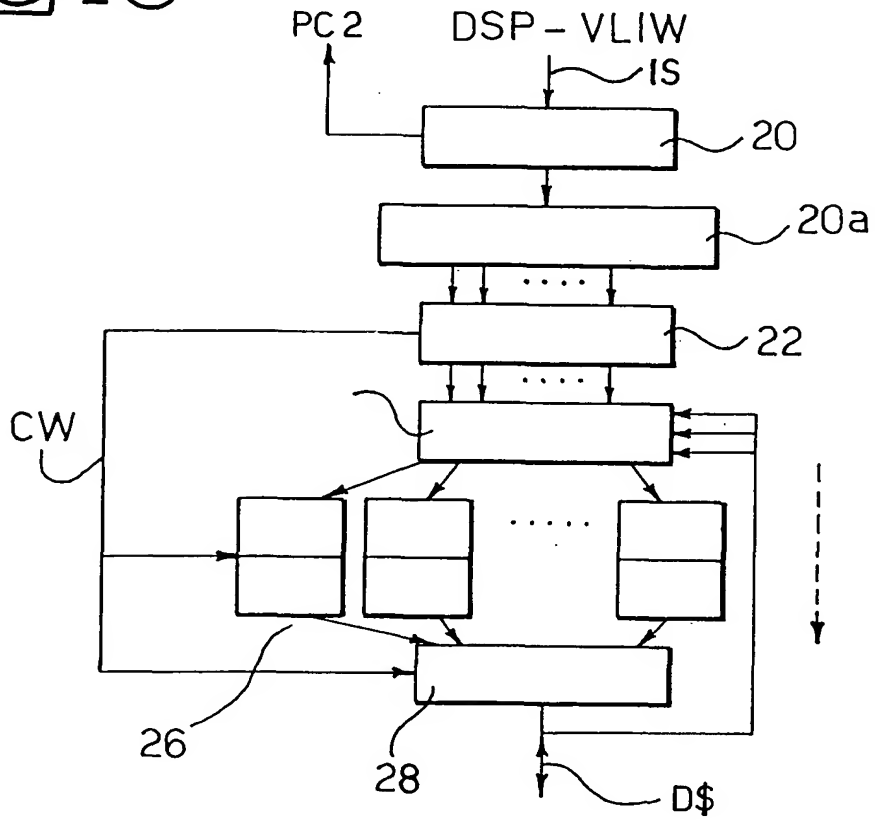
PC2
DSP – VLIW
IS
20
20a
22
CW
26
28
D$

Fig_4

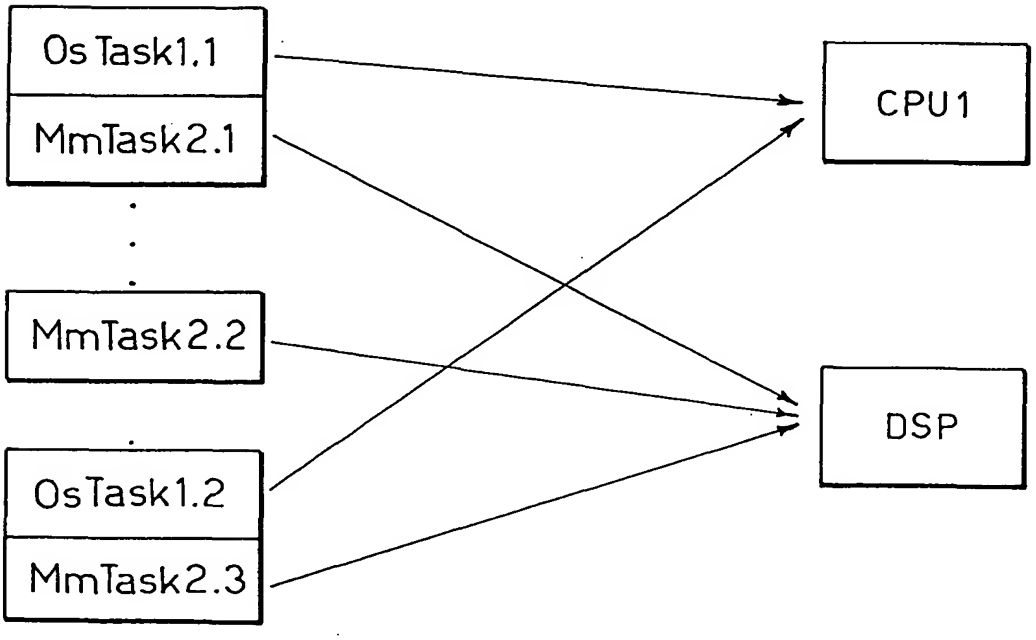
Os Task1.1
MmTask2.1
MmTask2.2
OsTask1.2
MmTask2.3
CPU1
DSP

Fig_5

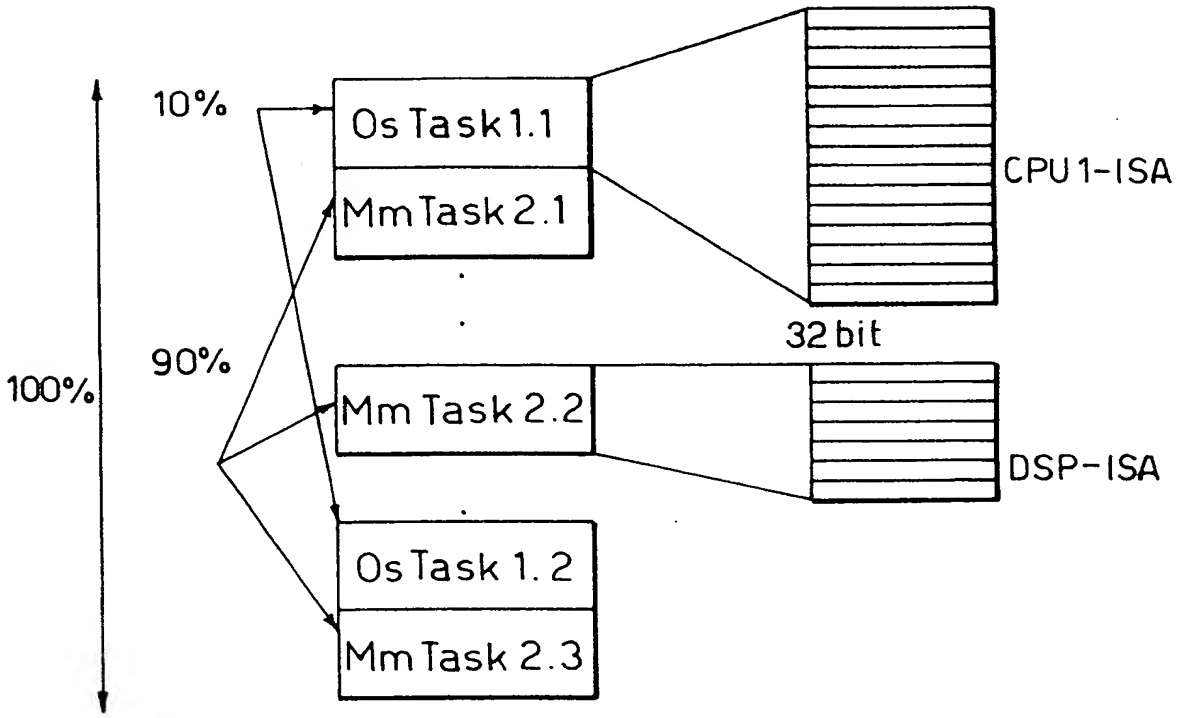
10%
90%
100%
Os Task 1.1
Mm Task 2.1
Mm Task 2.2
Os Task 1.2
Mm Task 2.3
CPU 1-ISA
32 bit
DSP-ISA

Fig_6

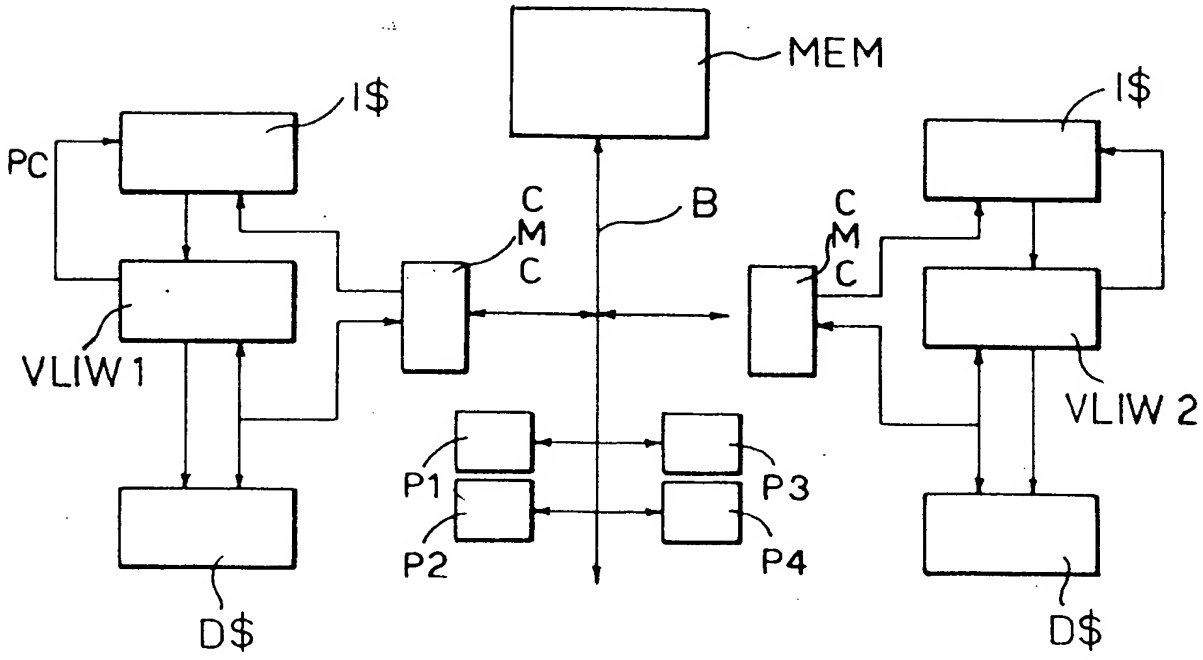
MEM
I$
PC
C
M
C
B
VLIW 1
P1
P2
P3
P4
D$
I$
C
M
C
VLIW 2
D$

Fig_7

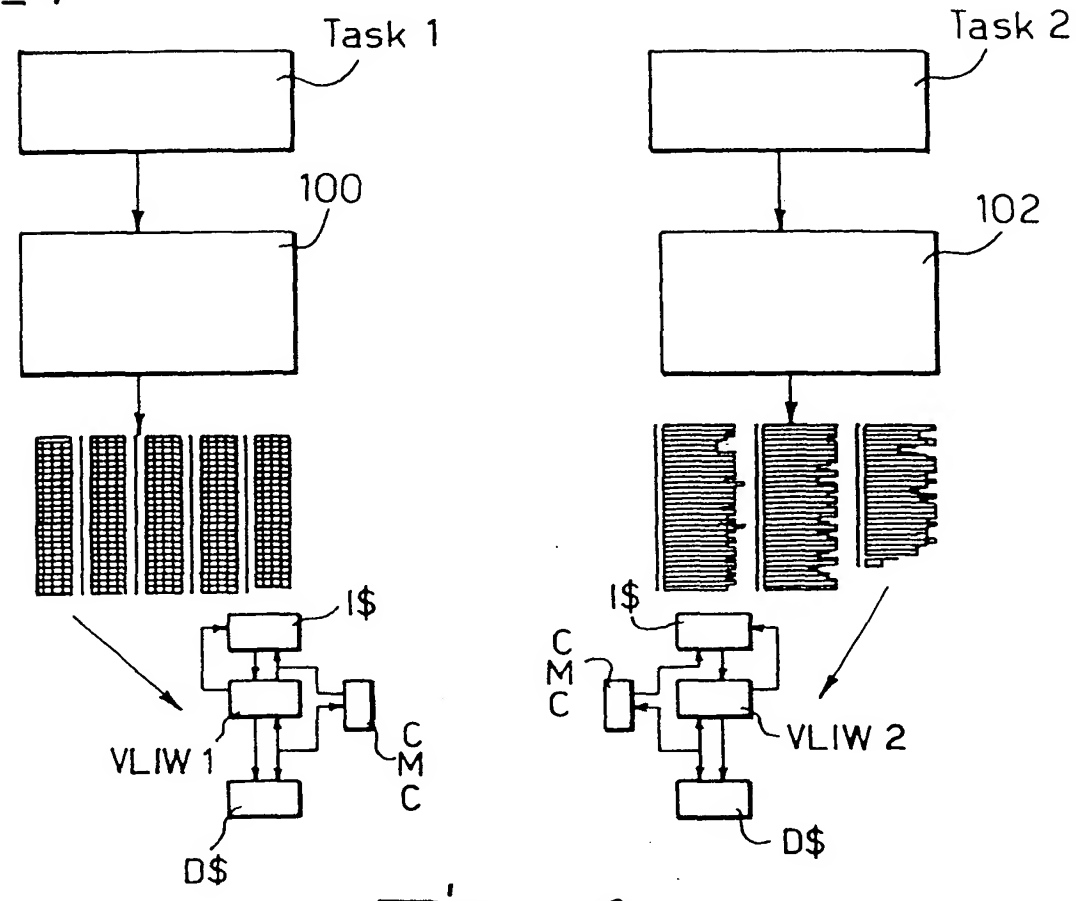
Task 1
Task 2
100
102
I$
I$
C
M
C
VLIW 1
C
M
C
VLIW 2
D$
D$

Fig_8

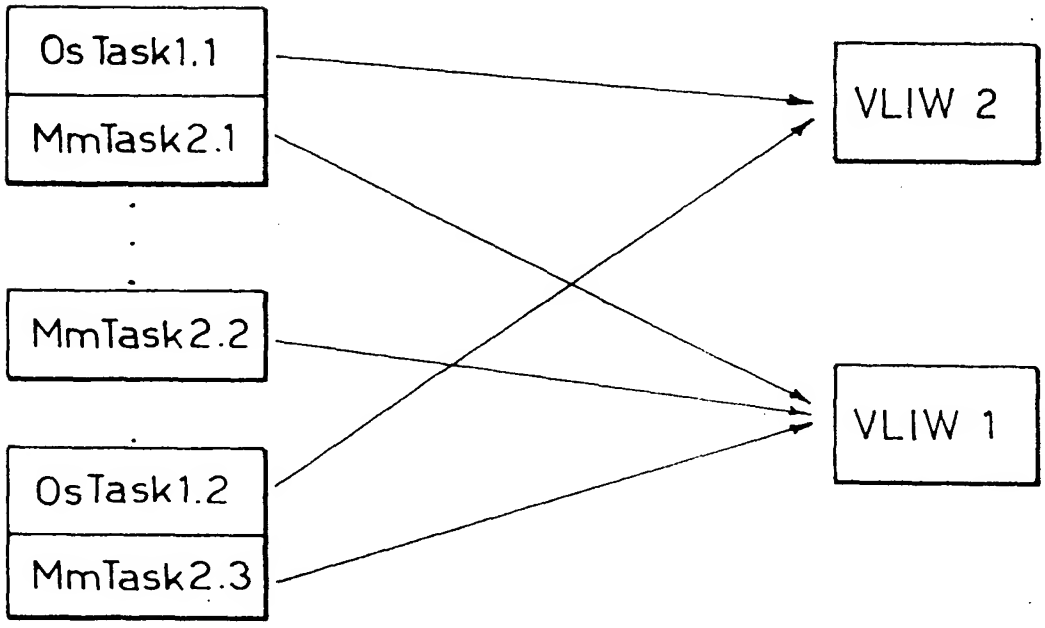
Os Task1.1
MmTask2.1
MmTask2.2
Os Task1.2
MmTask2.3
VLIW 2
VLIW 1

Fig_9

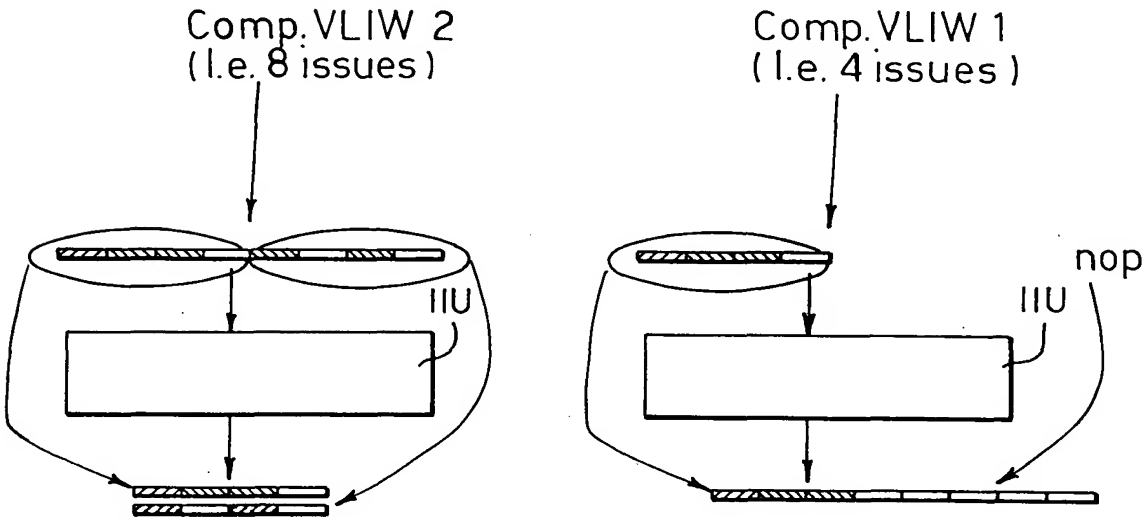
Comp. VLIW 2
(I.e. 8 issues)
Comp. VLIW 1
(I.e. 4 issues)
IIU
IIU
nop

Fig_10

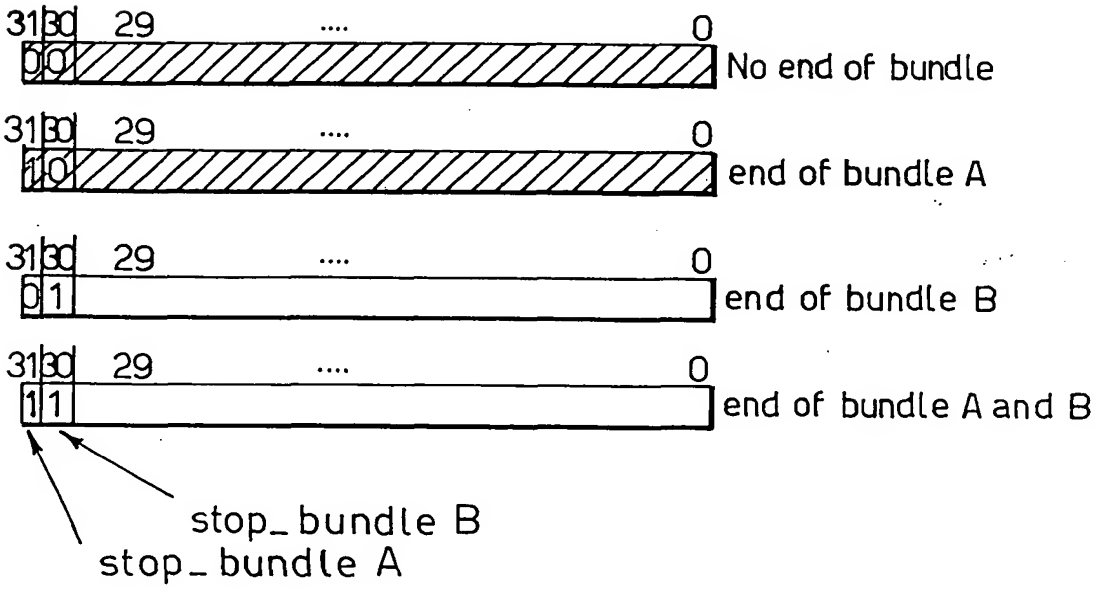
31 30 29 0
0 0
No end of bundle
31 30 29 0
1 0
end of bundle A
31 30 29 0
0 1
end of bundle B
31 30 29 0
1 1
end of bundle A and B
stop_bundle B
stop_bundle A

Fig_11

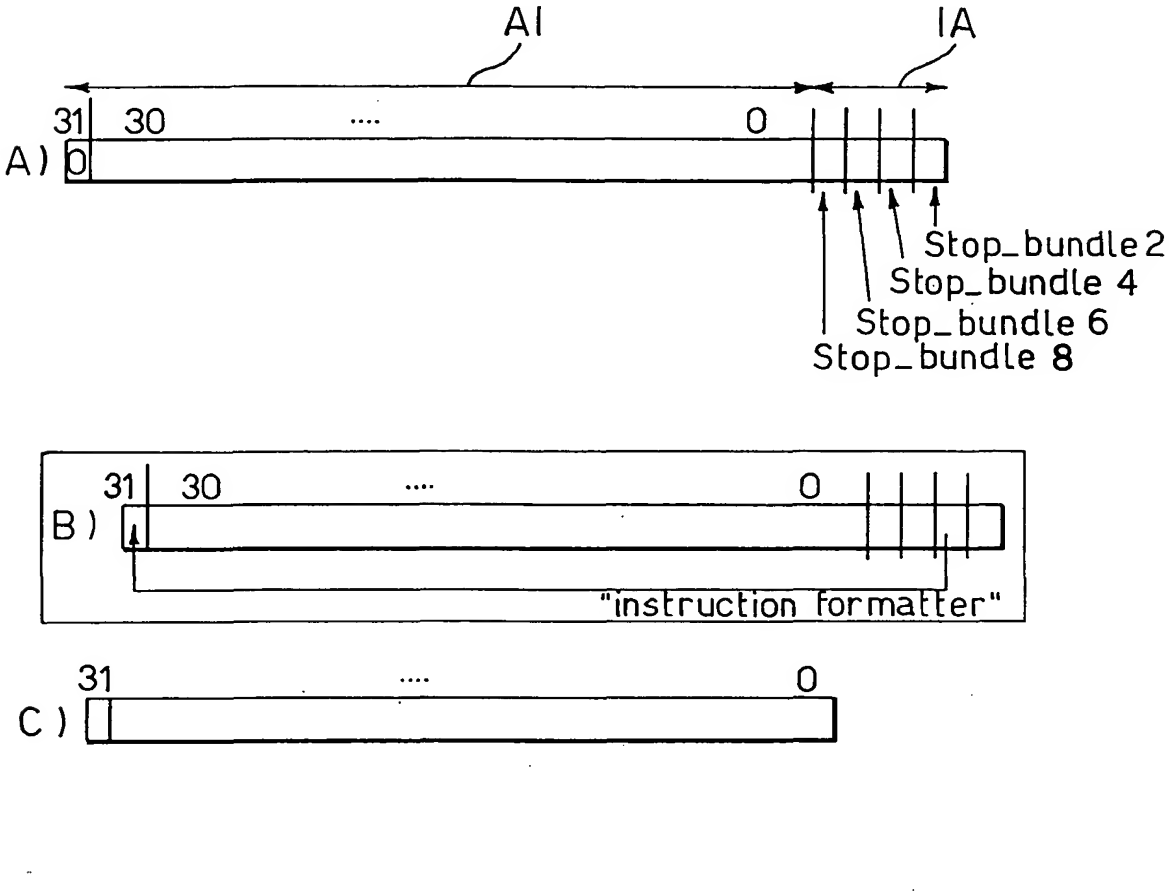
AI
IA
31
30
....
0
A)
Stop_bundle 2
Stop_bundle 4
Stop_bundle 6
Stop_bundle 8
B)
"instruction formatter"
C)

Fig_12

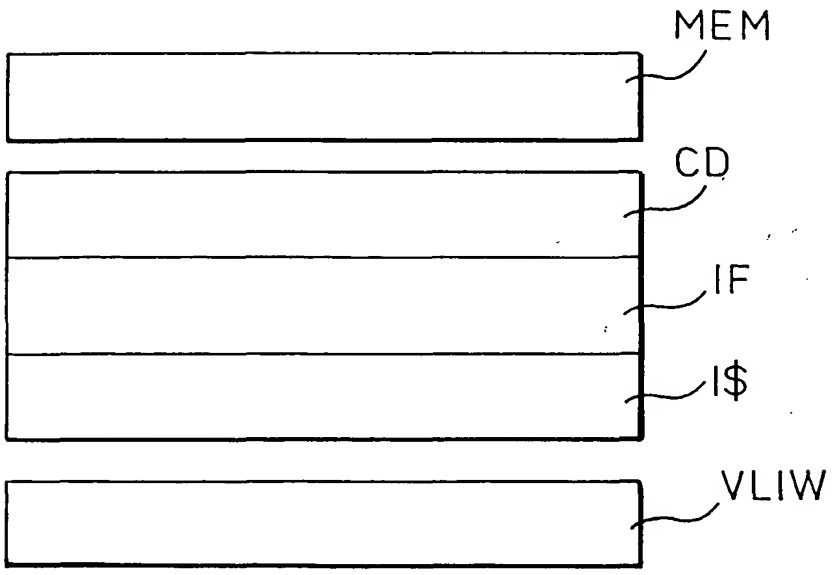
MEM
CD
IF
I$
VLIW

Fig_13

Process	Num.	%VLIW	Exec. time	Memory	Compiled Execution For VLIW Of Length	Compiled Execution On VLIW Of length	Memory address
SystemIdleProcess	0	52	4:18:39	16K	4	4	x1234123A
System	2	02	0:00:37	200K	8	8	x3E586321
SMSS.EXE	26	00	0:00:00	0K	4	8	xFFC0A867
CSRSS.EXE	34	00	0:00:06	908K	4	4	xAFE25432
WINLOGON.EXE	40	00	0:00:01	32K	8	4	xCECC4223
SERVICES.EXE	43	00	0:00:01	1044K	8	4	

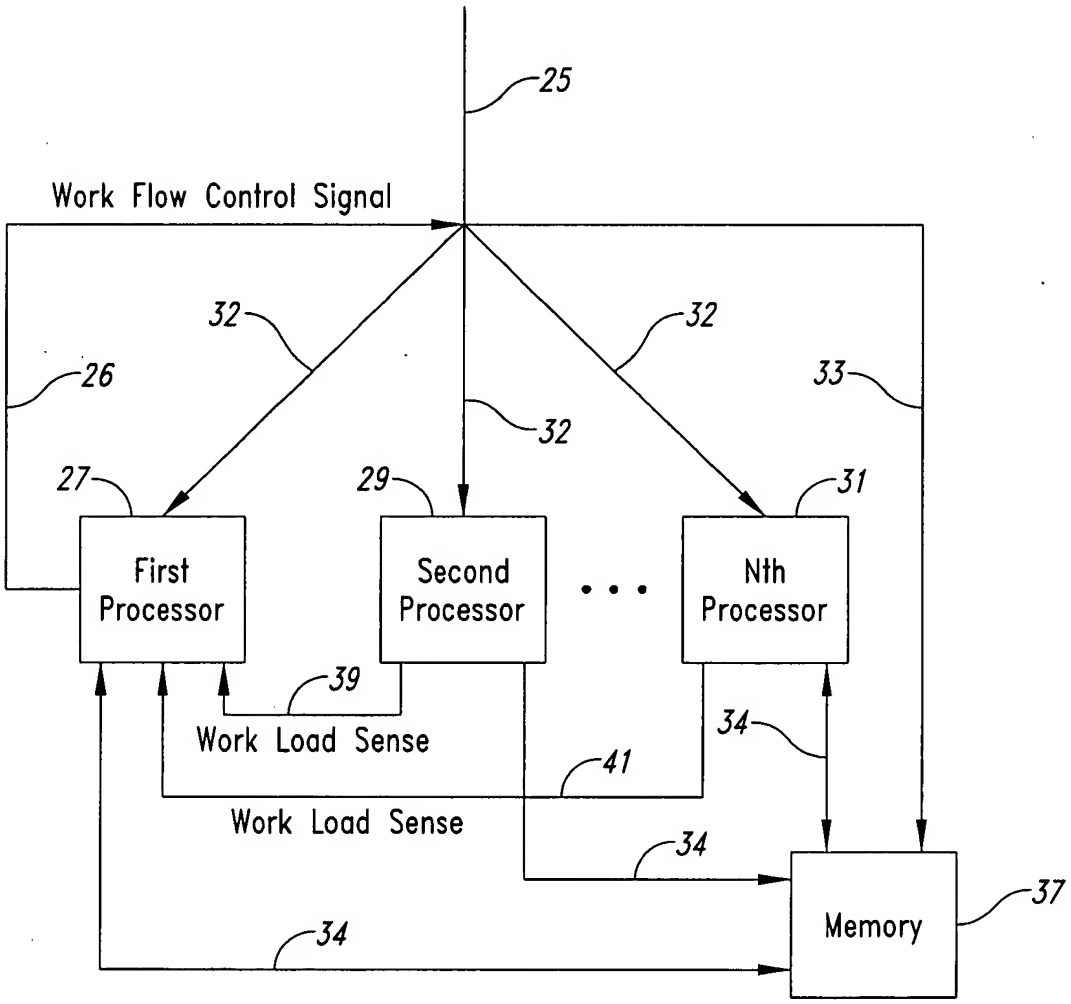
25
Work Flow Control Signal
32
32
32
26
33
27
29
31
First Processor
Second Processor
Nth Processor
39
Work Load Sense
34
41
Work Load Sense
34
34
Memory
37

FIG. 14